REMARKS

In accordance with the foregoing, claims 1-18 are pending, and it is respectfully submitted that the application is in condition for allowance. No new matter is presented in this Response.

REJECTIONS UNDER 35 U.S.C. §103:

Claims 1-2, 5-6, 8-10, and 11-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Inoue (U.S. Patent 5,696,774) in view of Arai (U.S. Patent 5,757,824) and further in view of Applicant admitted Prior Art (APA).

Claims 1-2

It is respectfully submitted that the Examiner has not shown where the prior art discloses each and every limitation recited in claims 1 and 2.

Error Flag Generator

Although the Examiner has asserted that Arai discloses the error flag generator recited by claim 1, it is respectfully submitted that the error flag generator disclosed by Arai is patentably distinct from the error flag generator recited by claim 1. "To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." MPEP 2143.03. The Examiner appears to make a *prima facie* case of obviousness by arguing that the error flag generator 57 disclosed in FIG. 17 of Arai teaches or suggests the error flag generator recited by claim 1, but in fact, the error flag generator 57 does not teach or suggest the error flag generator recited by claim 1.

Claim 1 recites:

> "...an error flag generator, which generates one of the error flags indicating an error existence/absence for a corresponding one of the ECC data blocks with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory (emphasis added)."

At page 3 of the Office Action, the Examiner contends that "Arai (fig. 17 shows a code error correction apparatus including an error flag generator (57), which generates an error flag

indicating an error existence/absence for ECC (Error-Correction Coding) data (col. 12, lines 66 through col. 13 line 6)." However, Arai does not disclose an error flag generator which generates an error flag indicating an error existence/absence for a corresponding one of the ECC data blocks with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory, as recited by claim 1. The error flag generator 57 disclosed by Arai only uses error flags read out from an error flag memory 38. Arai, col. 13, lines 3-6; FIG. 17.

The specification of Arai does not disclose a frame-sync error memory, does not disclose frame-sync error information read from a frame-sync error memory, and does not disclose an error flag generator which generates an error flag with reference to frame-sync error information. Furthermore, FIG. 17 does not disclose a frame-sync error memory of any kind. The error flag generator 57 disclosed by Arai only generates an error flag based on error flags read out from an error flag memory 38.

Additionally, Arai does not suggest the error flag generator recited in claim 1. The specification of Arai does not once mention frame-sync error information. There is no suggestion in Arai to use the error flag generator 57 to generate error flags using any kind of information other than the error flag read out from the error flag memory 38. FIGs. 1-17 do not in any way suggest generating an error flag using frame-sync error information. Thus, it is respectfully submitted that Arai does not suggest the error flag generator recited in claim 1.

For these reasons, it is respectfully submitted that the rejection of claim 1 should be withdrawn.

Frame-Sync Error Memory

Furthermore, although the Examiner has cited to the frame sync data disclosed by the APA is support of the assertion that the APA discloses the frame-sync error memory recited by claim 1, it is respectfully submitted that the frame-sync data disclosed by APA is patentably distinct from the frame-sync error memory recited by claim 1. Claim 1 recites: "...a frame-sync error memory which stores frame-sync error information for at least one of the ECC data blocks."

At page 3 of the Office Action, the Examiner argues that "Inoue does not explicitly disclose a frame-sync error memory which stores frame-sync error information for at least one data block. However, the limitation is obvious and very well known in the art, as evidenced by APA (see specification [0006]-[0007], fig. 1)."

Paragraphs [0006]-[0007] and fig. 1 of the instant application disclose frame-sync data,

not a frame-sync error memory. Frame-sync data is information itself, whereas a frame-sync error memory is a structural component which stores error information about a frame. Thus, the APA does not disclose the frame-sync error memory recited by claim 1. Accordingly, it is respectfully submitted that the rejection of claim 1 should be withdrawn for at least this reason as well.

Regarding claim 2, it is respectfully submitted that claim 2 is patentable for at least the same reasons that claim 1 is patentable.

Claims 5 and 6

The Examiner has not shown where the prior art discloses each and every limitation recited in claims 5 and 6.

Generating Error Flags

Although the Examiner has asserted that Arai discloses the operation of generating error flags recited by claim 5, it is respectfully submitted that the operation of generating error flags disclosed by Arai is patentably distinct from the operation of generating error flags recited by claim 5. "To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." MPEP 2143.03. The Examiner appears to make a *prima facie* case of obviousness by arguing that the operation of the error flag generator 57 disclosed in FIG. 17 of Arai generating error flags teaches or suggests the operation of generating error flags generator recited by claim 5, but in fact, the operation of the error flag generator 57 generating error flags does not teach or suggest the operation of generating error flags recited by claim 5.

Claim 5 recites:

> "...generating error flags indicating error existence/absence for a corresponding ECC data block with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory (emphasis added)."

Arai does not disclose the operation of generating error flags indicating error existence/absence for a corresponding ECC data block with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory, as recited by claim 5. The error flag generator 57 disclosed by Arai only uses error

flags read out from an error flag memory 38. Arai, col. 13, lines 3-6; FIG. 17.

The specification of Arai does not disclose a frame-sync error memory, does not disclose frame-sync error information read from a frame-sync error memory, and does not disclose generating an error flag with reference to frame-sync error information. Furthermore, FIG. 17 of Arai does not illustrate frame-sync error memory of any kind.

Additionally, Arai does not suggest the operation of generating error flags recited in claim 5. The specification of Arai does not once mention frame-sync error information. There is no suggestion in Arai to generate error flags using any kind of information other than the error flag read out from the error flag memory 38. FIGs. 1-17 do not in any way suggest generating an error flag using frame-sync error information. Thus, it is respectfully submitted that Arai does not suggest the operation of generating error flags recited in claim 5.

For these reasons, it is respectfully submitted that the rejection of claim 5 should be withdrawn.

Frame-Sync Error Memory

Furthermore, as explained above with reference to claim 1, the Examiner incorrectly asserts that the frame-sync data disclosed by the APA reads on the frame-sync error memory recited by claim 5. Frame-sync data is information itself, whereas a frame-sync error memory is a structural component which stores error information about a frame. Thus, the APA does not disclose the frame-sync error memory recited by claim 5.

Regarding claim 6, it is respectfully submitted that claim 6 is patentable for at least the same reasons that claim 5 is patentable.

Based on the foregoing, this rejection is respectfully requested to be withdrawn.

Claims 8-10 and 11-17

It is respectfully submitted that the Examiner has not shown where the prior art discloses each and every limitation recited in claims 8-10 and 11-17.

Error Flag Generator

Although the Examiner has asserted that Arai discloses the error flag generator recited by claim 8, it is respectfully submitted that the error flag generator disclosed by Arai is patentably distinct from the error flag generator recited by claim 8. "To establish *prima facie* obviousness of

a claimed invention, all the claim limitations must be taught or suggested by the prior art." MPEP 2143.03. The Examiner appears to make a *prima facie* case of obviousness by arguing that the error flag generator 57 disclosed in FIG. 17 of Arai teaches or suggests the error flag generator recited by claim 8, but in fact, the error flag generator 57 does not teach or suggest the error flag generator recited by claim 8.

Claim 8 recites:

> "...an error flag generator, generating one of the error flags indicating an existence/absence of an error for a corresponding one of the ECC data blocks with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory (emphasis added)."

At page 4 of the Office Action, the Examiner argues that "as to claim 8, the claim differs from claim 1 by the additional limitation 'a frame-sync detector, outputting frame-sync error information indicating an existence/absence of an error for frame sync-data of frames forming the ECC data blocks.' However, the limitation is clearly disclosed by APA (see specification [0006-0007], fig. 1."

Arai does not disclose the error flag generator recited by claim 8. The error flag generator 57 disclosed by Arai only uses error flags read out from an error flag memory 38. Arai, col. 13, lines 3-6; FIG. 17. In contrast, the error flag generator recited by claim 8 generates an error flag with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory. The specification of Arai does not disclose a frame-sync error memory, does not disclose frame-sync error information read from a frame-sync error memory, and does not disclose an error flag generator which generates an error flag with reference to frame-sync error information. Furthermore, FIG. 17 of Arai does not illustrate a frame-sync error memory of any kind.

Additionally, Arai does not suggest the error flag generator recited in claim 8. The specification of Arai does not once mention frame-sync error information. There is no suggestion in Arai to use the error flag generator 57 to generate error flags using any kind of information other than the error flag read out from the error flag memory 38. FIGs. 1-17 do not in any way suggest generating an error flag using frame-sync error information. Thus, it is respectfully submitted that Arai does not suggest the error flag generator recited in claim 8.

For these reasons, it is respectfully submitted that the rejection of claim 8 should be

withdrawn.

Frame-Sync Error Memory

Furthermore, as explained above with reference to claim 1, the Examiner has not shown where the prior art discloses the frame-sync error memory recited by claim 8.

Frame-Sync Detector

Additionally, the Examiner has not shown where the prior art discloses the frame-sync detector recited by claim 8. The Examiner argues that the frame-sync detector is "clearly disclosed by APA (see specification [0006-0007], fig. 1)."

Paragraphs [0006]-[0007] and fig. 1 of the instant application disclose frame-sync data, not a frame-sync error memory. Frame-sync data is information itself, whereas a frame-sync detector is a structural component which detects frame-sync information. Thus, the APA does not disclose the frame-sync detector recited by claim 8. Accordingly, it is respectfully submitted that the rejection of claim 8 should be withdrawn for at least this reason as well.

Regarding claims 9, 10, and 11-17, it is respectfully submitted that claims 9, 10, and 11-17 are patentable for at least the same reasons that claim 8 is patentable.

ALLOWABLE SUBJECT MATTER:

Claims 3-4, 7 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

CONCLUSION:

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

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